REMARKS

Reconsideration and allowance in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-6 remain pending in the application.

Applicant appreciatively notes that claims 1-3 and 6 are allowable.

Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Theil et al (6,396,118). Applicant respectfully traverses this rejection.

An Information Disclosure Statement is being submitted concurrently herewith providing documents cited during examination of the PCT Application.

Applicant respectfully submits that the Examiner makes an incorrect interpretation of each of these prior art documents. Regarding Theil, the Examiner indicates that the prior art structure discloses conductive vias between electrical contacts on the back of the chip and contact lands on the front of the chip, for access to the matrix array. It is assumed that the Examiner refers to conductive vias 212, 214, 216, 218 in Figure 2, for instance. However, the Examiner may have been deceived by the scale of the Figures, such as Figure 2 in Theil, it seems that the Examiner has considered layer 210 as the substrate or the chip, which it is not the case. In Figure 2 for instance, interconnection structure 2310 may look like a chip substrate; but it is not a chip substrate. In fact, structure 210 is a classical interconnect structure, i.e. a stack of insulating and conductive layer deposited on substrate 200; it is at most a few micrometers thick, whereas the actual substrate (200) is a few hundred micrometers thick.

In the claimed invention, the conductive vias go through the chip substrate from the back side to the front side. In Theil, the conductive vias remain on the front side and there are no electrical contacts on the back side and no conductive vias through the substrate.

Therefore, although classical interconnect vias are provided in Theil through the deposited insulating layer, there is no suggestion for conductive vias going from the front face to the back face of the chip. No electrical contact lands are provided on the back face, as can easily be seen in the figures of Theil. For at least these reasons, claim 4 is not anticipated by Theil and

accordingly, the rejection should be withdrawn.

Claims 4 and 5 are rejected under 35 U.S.C. 102(a) as being anticipated by Tao (US 2003/0214618). Applicant respectfully traverse this rejection.

Concerning US 2003/0214618 to Tao et al., it is clear that there is no conductive vias through the thickness of the substrate for connecting electrical land contacts on the front face of the chip to electrical contacts on the back side of the chip. Therefore, it is not understood why the Examiner states that those are known from Tao et al. Accordingly, the anticipation rejection should be withdrawn.

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

Early issuance of a Notice of Allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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